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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/659,210	09/09/2003	Joseph C. Fjelstad	SIPI.P108	5685

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Law Office of Ronald Shea
2540 Country Hills Rd
Apt. 192
Brea, CA 92821

EXAMINER	
SEMENENKO, YURIY	
ART UNIT	**PAPER NUMBER**
2841	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/659,210	FJELSTAD ET AL.	
	Examiner	Art Unit	
	YURIY SEMENENKO	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Amendment at 11/26/2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-29 and 84-98* is/are pending in the application.

4a) Of the above claim(s) *3-29* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 84-98* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1 Claims 1 and 94 are objected to because of the following informalities:

Claims 1 and 94: "a first daughter boards " and "a second daughter boards" should be changed to – the first daughter boards - and - the second daughter boards – respectively for proper antecedence basis.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

2.1. Claims 1, 84, 86, 89-98 are rejected under 35U.S.C. 103(a) as being unpatentable over Admitted by Applicant Prior Art, [hereinafter APA] in view of Plonski (Patent # 4679321) [hereinafter Plonski] and in view of Snyder et al. (Patent #5046966) hereinafter Snyder.

As to claim 1: APA discloses in Fig. 1 (Specification, page 1) an assembly 100 for forming a high speed signal path between first 103A and second 103B daughter boards, the assembly comprising: a substrate 101 having first and second surfaces; a first daughter boards 103A disposed proximate the first surface of the substrate 101; a second daughter boards 103B disposed proximate the first surface of the substrate 101; first 111A and second 111B through-holes within the substrate 101, each through-hole having a first opening at the first surface and a second opening at the second surface; a first conductive element (conductive wall of the first through-hole 111A) disposed within the first through-hole 111A and extending from the first surface to the second surface to form a first conductive via having first and second ends; a second conductive element (conductive wall of the second through-hole 111B) within the second through-hole 111B and extending from the first surface to the second surface to form a second conductive via having first and second ends; a first signal path electrically coupling the first daughter board 103A to the first conductive element in the first through-hole111A; a second signal path electrically coupling the second daughter board 103B to the second conductive element in the second through hole 111B,

except, APA doesn't explicitly teach two things:

1. an electronic cable having a first end and a second end, the first end of the electronic cable being inserted into the second end of the first via; and the second end of the electronic cable being inserted into the second end of the second via.
2. the first end of the electronic cable being in electrical contact with the first conductive via, and the second end of the electronic cable being in electrical contact with the second conductive via.

Plonski discloses in Fig. 2 an electronic cable 212 having a first end and a second end, the first end of the electronic cable being inserted into the first end of the first via (close to 205, column 4, lines 9-11) of the substrate 201; and the second end of the electronic cable 212 being inserted into the first end of the second via (close to 202).

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, to make the assembly, as taught by APA, with an electronic

cable having a first end and a second end, the first end of the electronic cable being inserted into the second end of the first via; and the second end of the electronic cable being inserted into the second end of the second via, as taught by Plonski, in order to provide preferred medium for high speed signals, as taught by Plonski (column 1, lines 23-27).

Snyder discloses in Fig. 1 the first end 31' of the electronic cable 11 being in electrical contact with the first conductive via 17 (column 3, lines 6-11).

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, to make the assembly, as taught by APA, with the first end of the electronic cable being in electrical contact with the first conductive via, and the second end of the electronic cable being in electrical contact with the second conductive via, as taught by Snyder, in order to provide electrical connections with the motherboard.

As to claim 84: APA and Plonski and Snyder disclose the assembly having all of the claimed features as discussed above with respect claim 1,

except APA and Plonski and Snyder do not explicitly teach the electronic cable is selected from among a group of cables consisting of single conductor cables and dual-conductor cables, and combinations thereof.

Plonski discloses in Fig. 1B the electronic cable 110 is of single conductor 116 cables.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, to make the electronic cable, as taught by APA and Plonski and Snyder, as a single conductor cables and, as taught by Plonski, in order to provide preferred medium for high speed signals, as taught by Plonski (column 1, lines 23-27).

As to claim 86: APA and Plonski and Snyder disclose the assembly having all of the claimed features as discussed above with respect claim 1,

except , APA and Plonski and Snyder do not explicitly teach the first end of the electronic cable is electrically coupled to the first via proximate the first opening of the first through-hole to mitigate signal reflection.

Snyder discloses in Fig. 1 the first end 31 of the first electronic cable 11 is electrically coupled to the first via 17 proximate the first opening of the first through-hole to mitigate signal reflection.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, to make the first end of the electronic cable, as taught by APA and Plonski and Snyder is electrically coupled to the first via proximate the first opening of the first through-hole to mitigate signal reflection, as taught by Snyder, in order to provide densely packaged electrical connection, as taught by Snyder (column 1, lines 60-65).

As to claim 89: APA and Plonski and Snyder disclose the assembly having all of the claimed features as discussed above with respect claim 1, wherein the substrate 101, Fig. 1 comprises a plurality of layers (Specification , page 2, [0004]).

As to claim 90: APA and Plonski and Snyder disclose the assembly having all of the claimed features as discussed above with respect claim 1,herein the substrate comprises at least one conductive, 113, Fig. 1, (Specification , page 2, [0004]).

As to claims 91 and 92: APA and Plonski and Snyder disclose the assembly having all of the claimed features as discussed above with respect claim 90,

except APA and Plonski and Snyder do not teach said at least one conductive trace includes a conductive trace coupled to ground potential or to source voltage.

Snyder discloses in Fig. 1 said at least one conductive trace 15 includes a conductive trace coupled to ground potential (column 3, lines 51-59) or to source voltage (column 3, lines 21-29).

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, to make said at least one conductive trace, as taught by APA

and Plonski and Snyder, including a conductive trace coupled to ground potential, as taught by Snyder in order to provide proper electrical grounding for cables, as taught by Snyder (column 6, lines 5-9).

As to claim 93: APA and Plonski and Snyder disclose the assembly having all of the claimed features as discussed above with respect claim 1,

except APA and Plonski and Snyder do not explicitly teach the first end of the electronic cable is secured within the first conductive via by a securing engagement selected from among a plurality of securing engagements consisting of solder, press fitted ends, frictionally secured ends, retaining hardware, and combinations thereof.

Snyder discloses in Fig. 1 the first cable end 31 is secured within the first conductive via 17 by a securing engagement is pin 31' – socket member 51 (column 5, lines 15-29)

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, to make the first end of the electronic cable, as taught by APA and Plonski and Snyder, ~~is~~ secured within the first conductive via by a securing engagement which are press fitted ends, as taught by Snyder, in order to provide robust electrical connection.

As to claim 94: APA discloses in Fig. 1 (Specification, page 1) an assembly 100 for forming a high speed signal path between first 103A and second 103B daughter boards, the assembly comprising: a substrate 101 having first and second surfaces; a first daughter board 103A disposed proximate the first surface of the substrate 101; a second daughter board 103B disposed proximate the first surface of the substrate 101; first 11A and second 111B through-holes within the substrate 101, each through-hole having a first opening at the first surface and a second opening at the second surface; a first conductive element (conductive wall of the first through-hole 111A) disposed within the first through-hole 111A and extending from the first surface to the second surface to form a first conductive via; a second conductive element (conductive wall of the first

through-hole 111B) within the second through-hole 111B and extending from the first surface to the second surface to form a second conductive via,

except, APA doesn't explicitly teach two things:

1. an electronic cable having a first end and a second end, the first end of the electronic cable being inserted into the second end of the first via; and the second end of the electronic cable being inserted into the second end of the second via.
2. the first end of the electronic cable being in electrical contact with the first conductive via, and the second end of the electronic cable being in electrical contact with the second conductive via.

Plonski discloses in Fig. 2 an electronic cable 212 having a first end and a second end, the first end of the electronic cable being inserted into the first end of the first via (close to 205, column 4, lines 9-11) of the substrate 201; and the second end of the electronic cable 212 being inserted into the first end of the second via (close to 202).

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, to make the assembly, as taught by APA, with an electronic cable having a first end and a second end, the first end of the electronic cable being inserted into the second end of the first via; and the second end of the electronic cable being inserted into the second end of the second via, as taught by Plonski, in order to provide preferred medium for high speed signals, as taught by Plonski (column 1, lines 23-27).

Snyder discloses in Fig. 1 the first end 31' of the electronic cable 11 being in electrical contact with the first conductive via 17 (column 3, lines 6-11).

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, to make the assembly, as taught by APA, with the first end of the electronic cable being in electrical contact with the first conductive via, and the second end of the electronic cable being in electrical contact with the second conductive via, as taught by Snyder, in order to provide electrical connections with the motherboard.

As to claim 95: APA and Plonski and Snyder disclose the assembly having all of the claimed features as discussed above with respect claim 1, wherein the first electronic member 103A, Fig. 1 comprises a first daughter board 119 having a conductive path conductively coupled to the first conductive via 111A.

As to claim 96: APA and Plonski and Snyder disclose the assembly having all of the claimed features as discussed above with respect claim 95 further comprising a conductive pin 123, Fig. 1 having first and second ends, the first end of the conductive pin sized to fit into the second end of the first through-hole 111A, and configured to electrically engage the first conductive via, and the second end of the pin conductively coupled to the first conductive path, Fig. 1 and Specification, page 1, [0004].

As to claim 97: APA and Plonski and Snyder disclose the assembly having all of the claimed features as discussed above with respect claim 96, wherein the daughter board 103A, Fig. 1 further comprises a conductive engagement member 105 for mechanically and electrically coupling the first conductive path to the conductive pin 123, the conductive engagement member 105 having a distal end coupled to the first conductive path, and a proximal end having a mechanical capture 121 to releasably engage to the second end of the conductive pin 123.

As to claim 98: APA and Plonski and Snyder disclose the assembly having all of the claimed features as discussed above with respect claim 95, further comprising an edge connector 105, Fig. 1 and (Specification, page 2, [0004]) with parallel first and second sides, the edge connector being secured to the substrate, wherein the first daughter board 103A (119) is fixably secured between the parallel first and second sides of the edge connector 105.

2.2. Claims 85, 87 and 88 are rejected under 35 U.S.C. 103(a) as being unpatentable over APA in view of Plonski and in view of Snyder, as applied to claims 1, 84, 86, 89-98 above, and further in view of Kuczynski (Patent #6218621) [hereinafter Kuczynski].

As to claims 85, 87 and 88: APA and Plonski and Snyder disclose the assembly having all of the claimed features as discussed above with respect claim 1,

except APA and Plonski and Snyder do not teach the electronic cable is selected from among a group of dual-conductor cables consisting of twin-axial cables, coaxial cables, twisted pair cables, and combinations thereof, and wherein the dual conductor cable comprises a first conductor and a second conductor that are equal in length from respective first ends to respective second ends, and wherein the first ends of the first and second conductors of the dual conductor cable are cut perpendicular to their respective lengths.

Kuczynski discloses in Fig. 1 a dual conductor cable is twisted pair cables (column 4, lines 35-44), and wherein the dual conductor cable comprises first and second conductors that are equal in length from respective first ends to respective second ends, Fig. 2, and wherein the first ends of the first and second conductors of the dual conductor cable are cut perpendicular to their respective lengths, Fig. 2.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, to make the electronic cable, as taught by APA and Plonski and Snyder, as a twisted pair cables, and wherein the dual conductor cable comprises a first conductor and a second conductor that are equal in length from respective first ends to respective second ends, and wherein the first ends of the first and second conductors of the dual conductor cable are cut perpendicular to their respective lengths, as taught by Kuczynski, in order to provide high-frequency data transmission cable, as taught by Kuczynski (Abstract).

Response to Arguments

3. Applicant's arguments filed 11/26/2008 have been considered but they are not persuasive.

A. Applicants argument with respect to claims 1 and 94: "[b]ecause Plonski discloses a non-metalized hole, whereas APA and Snyder disclose a conductive via, any attempt

to combine these references would render them inoperable." This argument is not persuasive because modification by Plonski's reference provide an electronic cable 212, Fig. 2 being inserted into the first end of the first via (close to 205, column 4, lines 9-11) of the substrate 201. Such modification of APA's printed circuit board by added cables would provided preferred medium for high speed signals, as taught by Plonski (column 1, lines 23-27). What concern to through-holes, APA, not Plonski, clearly teaches first 111A and second 111B conductive vias extending from the first surface to the second surface of the substrate 101 (Specification, page 2, [0004]). The Applicants argue "because Plonski specifies un-metallized holes, and claim 1 recites conductive vias, Plonski is teaching away from claim one." Plonski is not teaching away from claims 1 and 94, but teaching another way to electrically connect coaxial conductor to the circuit board.

B. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, all of the references (APA, Plonski and Snyder) are analogous art because they are from the same field of the endeavor, (electrical assemblies).

C. In response to applicant's arguments with respect to claims 1 and 94 against the references individually, this argument is not persuasive because Applicant cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See In re Keller, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); In re Merck & Co., 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yuriy Semenenko whose telephone number is (571) 272-6106. The examiner can normally be reached on 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diego F. F. Gutiérrez can be reached on (571) 272-2245. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

YS

Diego Gutierrez
Supervisory Patent Examiner
Technology Center 2800